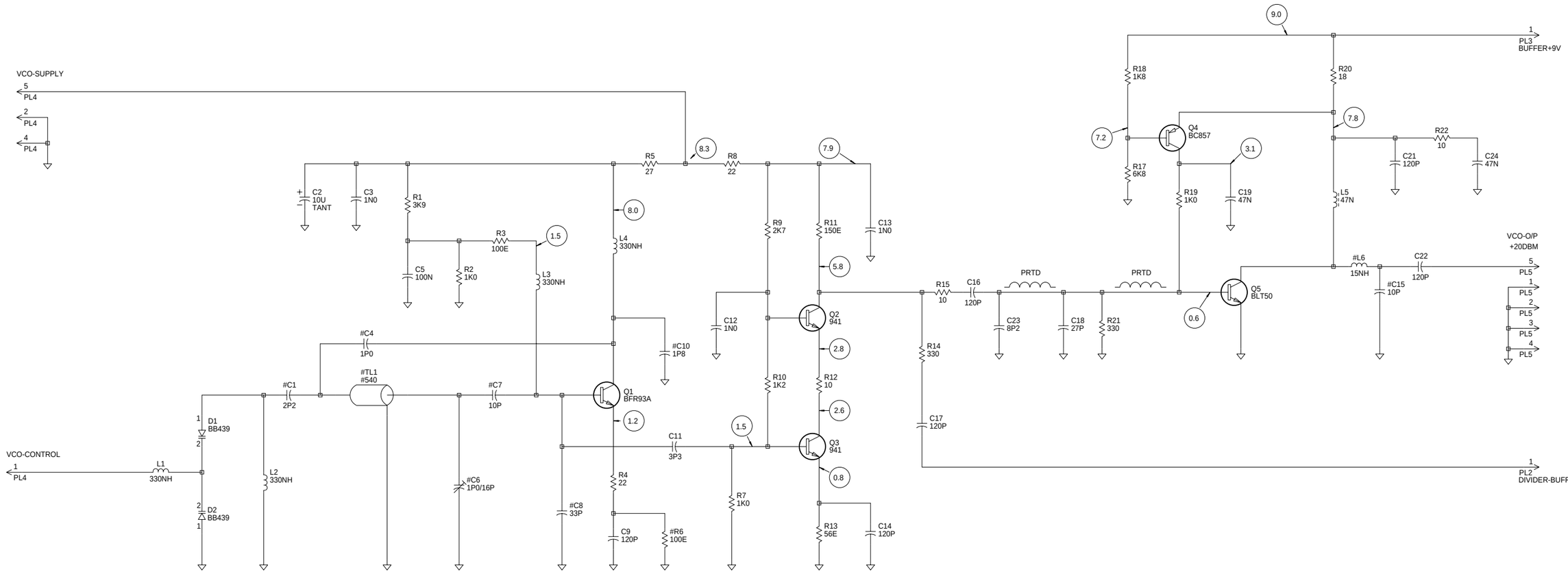


#-VALUE CHANGES FOR DIFFERENT OPTIONS

○ = D.C. CONDITIONS (VOLTS)
(USE HIGH IMPEDENCE PROBE)

PL5 5 PLUG PINS

PL4 5 PLUG PINS

PL2 1 PIN PLUG

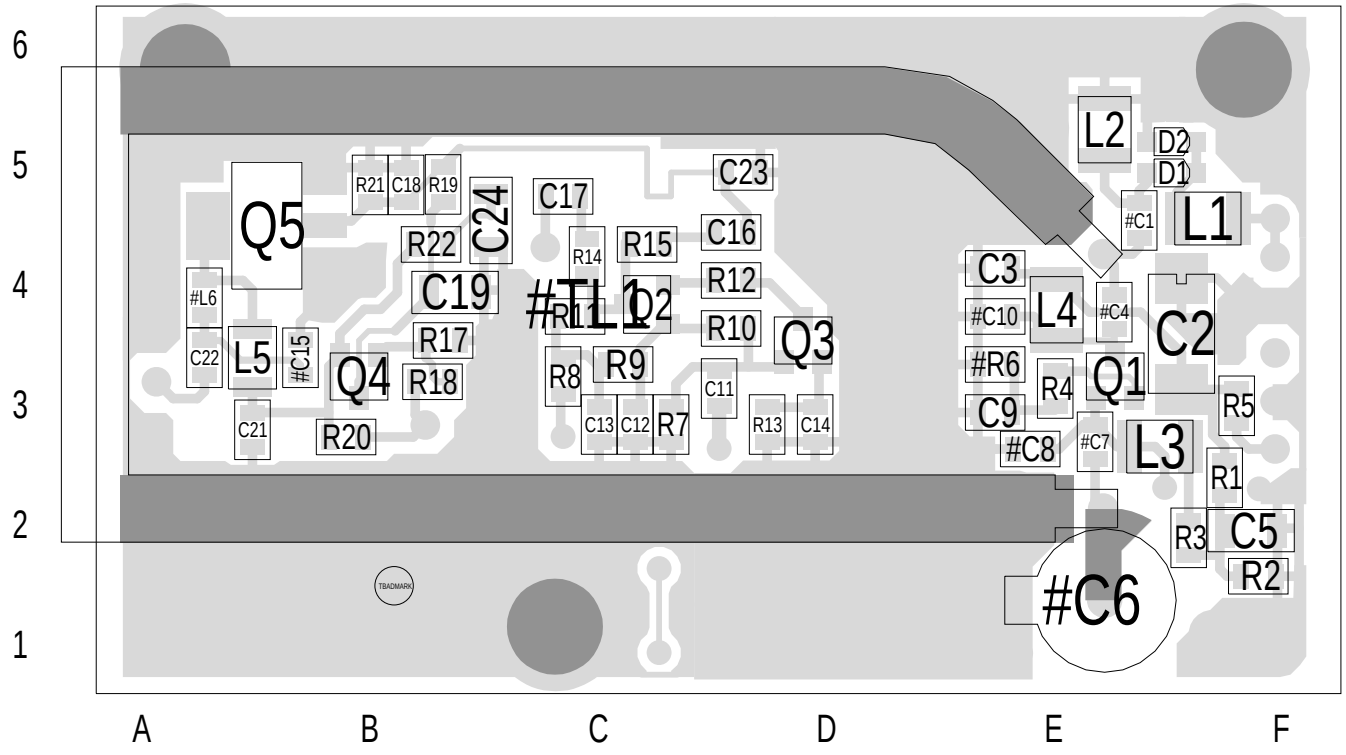
PL3 1 PIN PLUG

TBADMARK
BADMARK

REV/ISS	AMENDMENTS	DRAWN	CHKD	D.O.	APVD	DATE
07A	MINOR UPDATE TO THE LAYOUT	SSAHI				06-09-00
06A	MINOR UPDATE	SSAHI				06-07-00
05A	UPDATE	SSAHI				05-05-00
04A	SMD PARTS ADDED	BENC				07-10-99
03A	CYCLIC KEYING MODIFICATION	BENC				

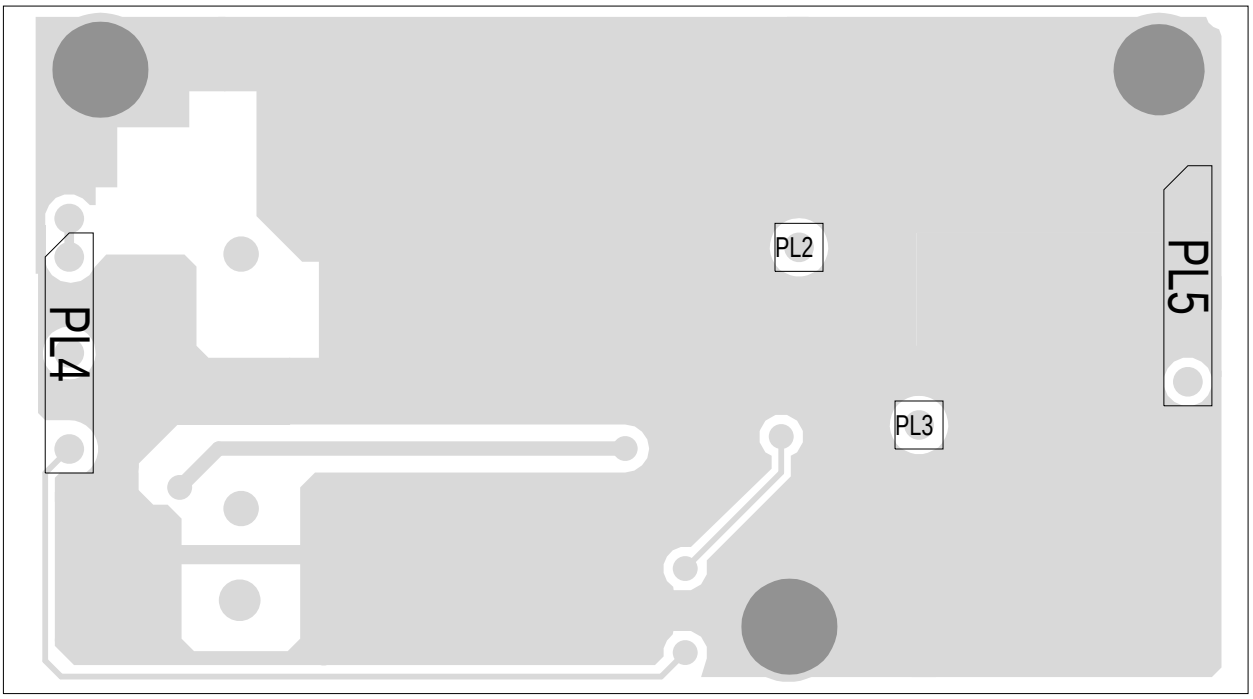
T850/T870 VCO

IPN:	ISSUE:	ID:		
220-01145-07	A	2.SC. 1		
PROJECT:	DESIGNER:	FILE NAME:	FILE DATE:	NO.SHEETS:
T850	SSAHI	1145_07a	6-Sep-00	1



TAIT ELECTRONICS	IPN: 220-01145-07	ISS: 07	ID: 1.TA	DATE: 6 Sep 2000
T850/T870VCO PCB LAYOUT - TOP SIDE				

Scale:2.5:1 ; Rotation: 0 degrees



6 5 4 3 2 1

F E D C B A

TAIT ELECTRONICS	IPN: 220-01145-07	ISS: 07	ID: 2.BA	DATE: 6 Sep 2000
T850/T870VCO PCB LAYOUT - BOTTOM SIDE				

Scale:2.5:1 ; Rotation: 0 degrees